REMARKS

Claims 3, 5, 6, 12, 13, 24, 26, 27, 33, 34, and 40-55 are presently pending in this application. Claims 3, 5, 6, 12, 13, 24, 26, 27, 33, and 34 have been amended to more particularly define the invention. Claims 1, 2, 4, 7-11, 14-23, 25, 28-32, and 35-39 have been canceled in the interest of expediting prosecution. Claims 40-55 have been added to assure Applicants the degree of protection to which their invention entitles them.

Claims 1-39 were rejected under 35 U.S.C. §102(e) as being anticipated by Shenoy, U.S. Patent No. 6,378,114. This rejection is respectfully traversed.

The claimed invention is directed to a method of and a system for modifying a plurality of domains of a circuit in a design space. The domains include at least one of a Boolean domain, an electrical domain, and a physical domain, and the circuit comprises a plurality of cells.

In accordance with exemplary embodiments of the method, as set forth, for example, in independent claims 40, 46, and 50, a possible netlist modification for the design space and a possible cell placement for the modified netlist are considered. These are not implemented at this time. It is determined whether the considered netlist modification and the considered cell placement improve the design space. If so, then the netlist modification and cell placement are implemented; but if not, a different netlist modification and cell placement are considered, and whether they improve the design space is determined. Accordingly, wasting of time, effort, and material in implementing unsatisfactory modifications and cell placements is avoided

The joint effect of two things is determined - - a modification to the netlist, and a cell placement for the modified netlist. They are always evaluated as a set, and if their joint effect is improvement of the design space, they are implemented as a set, but if the joint effect is not an improvement in the design space, they are not implemented, and instead a different modification and cell placement are considered, and their joint effect is determined.

Such a method and system are neither shown nor suggested by Shenoy. Accordingly, the claims are allowable.

In the exemplary embodiments of claims 12 and 33, at predetermined stages a determination is made of whether to intercept the method or process and implement the most recently considered netlist and cell placement. This is neither shown nor suggested by Shenoy. Accordingly, these claims are allowable for this further reason.

In the exemplary embodiments of claims 41 and 51, considering a cell placement comprises considering a plurality of placement techniques. Shenoy only uses partitioning to determine cell placement. Accordingly, claims 41 and 51 are allowable for this further reason.

The Examiner appears to feel that any decrease in a domain's level results in a failure of the proposed modification. This is not the case. For example, in a design space which has 10% spare space and timing just within the maximum desired, a netlist modification to add a gate and the resulting placement of that gate might reduce the spare space to 5% but improve the timing by 3ps. Although the Examiner might considered this modification a failure because it reduces the spare space, still the result meets the design performance criteria, and so the overall effect is an improvement in the design space.

Shenoy discloses a method for the placement of an integrated circuit. In his Figure 1 embodiment, Shenoy generates a netlist and performs cell placement. Then he executes cell separation. Once this is done, changes to the netlist are allowed. Spacing of the cells is then modified, and partitions are defined. If satisfactory convergence has been achieved, the process is completed; but if not, the process returns to the cell separation.

In Shenoy's Figure 3 embodiment, a mapped netlist is synthesized from user inputs, and cell separation is performed to assign coordinates for each cell. Partition walls are determined, and partitions formulated. Whether convergence has been achieved is then determined. If so, detailed placement is done; but if not, the method returns to cell separation.

In each Shenoy embodiment, cell placement is performed before a determination is made of whether convergence has occurred. Thus, if convergence is not satisfactory, the time, effort and expense of the cell placement is wasted.

In view of the foregoing, Applicant submits that claims 3, 5, 6, 12, 13, 24, 26, 27, 33, 34, and 40-55, all the claims presently pending in the application, are patentably distinct over the prior art of record and are allowable, and that the application is in condition for allowance. The Examiner is respectfully requested to pass the application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Attorney's Deposit Account No. 50-0481 and please credit any excess fees to such deposit account.

Respectfully Submitted,

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